REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

In the outstanding Office Action, Claims 1-13 were rejected under 35 U.S.C. §102(b) as anticipated by Sproch et al.

Turning now to the merits, Applicant's invention is directed to an information processing apparatus, as well as a method and computer storage medium relating thereto. As discussed in the Applicant's specification, conventional information processing apparatuses were problematic because synchronizing clock signals with variable frequency often leads to a pipeline design that operates primarily at the highest frequency of the signal.[1] Because of this particular design, lowered clock frequencies can appreciably reduce pipeline functionality through loss of processing performance and wasteful power consumption.[2]

Applicant's invention is directed to addressing this and/or other problems. Specifically, Claim 1 recites an information processing apparatus operating in synchronism with a synchronizing clock signal of a predetermined frequency. The apparatus includes a clock outputting means for varying the frequency of the synchronizing clock signal in order to output the synchronizing clock signal at the varied frequency. Also included is holding means for inputting and holding data when the clock outputting means outputs a first clock signal pulse, and further for outputting the data held therein when the clock outputting means outputs a second clock signal pulse following the first clock signal pulse. Selection command generating means is included for generating a selection command specifying whether or not to transfer the data by bypassing the holding means in accordance with the frequency of the synchronizing clock signal output by the synchronizing clock outputting means. A bypassing means outputs the data by bypassing the holding means if the selection

[1] Par. [0005], lines 1-4
[2] Par. [0005], lines 4-9

command generated by the selection command generating means specifies that the data be transferred by bypassing the holding means, and outputs the data output by the holding means if the selection command specifies that the data be transferred without bypassing the holding means. Furthermore, the synchronizing clock signal supplied to the holding means is cut off when the holding means is bypassed.

Thus, Claim 1 explicitly recites outputting a synchronized clock signal at a varied frequency and specifying whether or not to bypass the holding means in accordance with the frequency of synchronization clock signal output.

As noted above, a varying clock signal in an information processing method and apparatus often leads to poor processing performance as well as power inefficiencies, which the data bypass feature of the present invention addresses. However, the stall condition determination CKT of Sproch, et al. outputs a stall signal C based on comparison of sequential data signals, not based on frequency. Sproch, et al. is completely silent with respect to a varying clock frequency.

The outstanding Office Action attempts to correct this deficiency by stating that the varied clock frequency is inherent because the "clock CLK could be set to different clock frequencies."[3] However, it is settled law that "to establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill."[4] Moreover, "inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient."[5] While Sproch et al. discloses the use of a clock CLK, Appellants cannot find, and the Office Action does not provide, any evidence within Sproch et al. that demonstrates that it could or should

[3] OA at p2, lines 15-16
[4] In re Robertson 49 USPQ2d 1949, 1951 (Fed. Cir 1999)
[5] Continental Can Co. v. Monsanto Co., 948 F2d 1264, 1269, 20 USPQ2d 1746 (Fed. Cir. 1991)

be set to different frequencies, let alone that it *must* be set to different frequencies as required for inherency. The sole purpose of Sproch et al. is to use the clock to propagate data down a pipeline while also saving power through use of the stall signal C. In doing so, Sproch et al. does not require, mention, or seek to use the clock at varied frequencies as does Applicant's invention.

Further, Claim 1 recites bypassing the holding means if the selection command specifies that data be transferred by bypassing said holding means, and outputting the data output by the holding means if the selection command specifies that the data be transferred without bypassing the holding means. As discussed in Applicant's specification, this feature can allow for the data to either (1) travel directly *to* the holding means or (2) to *bypass around* the holding means and avoid it entirely.[6] That is, data propagation to the holding means without bypassing is performed every clock cycle, whereas data that bypasses moves past any designated bypassed holding means in a single clock cycle.[7] Page 25, line 20 to page 26, line 4 explains how this feature advantageously allows for appreciable power savings for the information processing apparatus, and page 47, line 16 to page 48, line 10, explains how this feature advantageously allows for a significant savings in processing time.

In contrast, the Sproch et al. invention discloses a way of saving power by clock gating certain stages of the pipeline as "inconsequential data" passes through the pipeline.[8] Unlike Applicant's invention, this inconsequential data does not avoid or bypass any registers but is simply maintained as the previous value in the register when the register is clock-gated.[9] Also unlike Applicant's invention, Sproch et al. requires continued clock cycles to propagate the "inconsequential data" through the pipeline and does not allow the data to pass through multiple stages on one clock cycle.

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[6] Fig. 4 of Applicant's Specification
[7] Figs. 12-13 of Applicant's Specification
[8] Sproch et al. at Col 9, lines 7-14 & lines 38-64
[9] Sproch et al. at Col 8, lines 59-61 stating "the stall signal, C, is propagated through the stages of the pipeline along with its associated inconsequential results"

More specifically, as seen in Fig. 5 of Sproch et al., consequential data (i.e., data that is different from a previous value) causes a logic high on the output of the Stall Condition "C" Determination Circuit 210. This enables AND Gate 351 such that the next clock signal is passed to the Register 221 and the consequential data is stored therein. Thereafter, if the Value Generator 207 generates inconsequential data (i.e., the same as a previous value), the Circuit 210 will output a low, which disables the AND Circuit 351 and blocks the subsequent clock signal from reaching the Register 221 so that the register "stores" the inconsequential data simply by maintaining the previous stored value. This low signal is also felt on the D input of the DQ Flip Flop 362, and passed to the Q output at the next clock cycle, which prevents the AND Gate 352 from sending the next clock signal to the Register 222. Thus, an inconsequential data value will set the "C" signal and this signal propagates through the DQ flip flops of the pipeline, which blocks the clock signals at each subsequent register such that the inconsequential data value propagates down the pipeline by maintaining a register value without clocking the register. This propagation of data *cannot* be said to bypass the registers/pipeline. Therefore, while Sproch et al. does help save power, it does not disclose a bypassing means element and subsequently does not result in significant savings in processing time as in Applicant's invention.

In view of the above-noted distinctions, Applicant respectfully submits that Claim 1 (and any claims dependent thereon) patentably distinguish over Sproch et al. Claims 7-9 (and any claims dependent thereon) recite elements analogous to those of Claim 1. Thus, Applicant respectfully submits that Claims 7-9 (and any claims dependent thereon) patentably distinguish over Sproch et al., for at least the reasons stated for Claim 1.

While Applicants believe that this response should result in allowance of this case, Applicants respectfully submit that since the present response traverses the prior art rejections

without substantive amendment, any new ground of rejection in a forthcoming office action ***will not be necessitated by amendment and cannot be properly made final.***[10]

Consequently, in light of the above discussion, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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[10] MPEP 706.07(a)